(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number : **0 338 766 B1**

(12) # EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification : **09.08.95 Bulletin 95/32**

(51) Int. Cl.[6] : **G02F 1/133,** H01L 21/84

(21) Application number : **89303812.5**

(22) Date of filing : **18.04.89**

(54) **Method of fabricating an active matrix substrate.**

(30) Priority : **20.04.88 JP 97008/88**
30.09.88 JP 248197/88

(43) Date of publication of application :
25.10.89 Bulletin 89/43

(45) Publication of the grant of the patent :
09.08.95 Bulletin 95/32

(84) Designated Contracting States :
DE FR GB

(56) References cited :
EP-A- 0 166 647
EP-A- 0 196 915
EP-A- 0 222 668

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EP 0 338 766 B1

Description

This invention relates to active matrix substrates for display devices used in liquid crystal television for video display, display for computer terminal or the like, and to methods for fabricating active matrix substrates for such use.

Recently, for the purpose of application into display devices, active matrix substrates for forming thin film transistors (TFTs) on a transparent substrate are being intensively developed. The structure of such active matrix substrates is explained by referring to FIG. 11. Numeral 1 is a TFT comprising a polycrystal silicon or amorphous silicon as a constituent element formed on a first transparent substrate (not shown), 2 is a liquid crystal between a transparent pixel electrode (electrically connected to the drain electrode of the TFT 1) and a transparent counter electrode on a second transparent substrate. 1 and 2 are disposed at a position corresponding to each pixel of a video display region 3, and it may be provided with, aside from the electrostatic capacity due to liquid crystal, a capacity formed in the active matrix substrate as storage capacity. Numeral 4 is gate bus line connected to the gate electrode of the TFT 1, and 5 is source bus line connected to the source electrode of the TFT 1. In FIG. 11, pixel electrodes, the TFTs, gate bus lines and source bus lines are formed on the first transparent substrate as an active matrix substrate.

An example of the construction of the TFT which is a constituent element of such active matrix substrate is described below with reference to FIG. 12. FIG. 12A is a plan view of the TFT possessing a inverted staggered structure, and FIG. 12B is an A-B sectional view of FIG. 12A. Numeral 6 is a transparent substrate made of glass, and 7 is a gate electrode. Numerals 9, 10, 11 are gate insulator layer (first insulator layer), first semiconductor layer and passivation layer, respectively. Numeral 8 is a silicon oxide layer for preventing contact between the gate electrode 7 and pixel electrode 15, and enhancing the adhesion between the gate insulator layer 9 and pixel electrode 15. Numerals 13 and 14 are drain electrode and source electrode, respectively. Numeral 12 is a second semiconductor layer for achieving an ohmic contact between the first semiconductor layer 10 and electrodes which are drain electrode 13 and source electrode 14. Numeral 15 is a transparent electrode connected to the drain electrode 13, and it is a pixel electrode for applying a voltage to the liquid crystal layer. In this example, meanwhile, the pixel electrode 15 is formed beneath the gate insulator layer 9, but this pixel electrode 15 may be also formed on the gate insulator layer, simultaneously and integrally with the drain electrode 13 and source electrode 14. Incidentally, in the TFT in the inverted staggered structure, since the gate electrode serves to shut off light against the incident light from the back side of the substrate, the leakage current in OFF state of TFT is small, and this structure is employed widely in commercial pocket-size TV sets.

A display device using such active matrix substrate is explained below while referring to FIG. 13. Between a counter substrate 17 to which a counter electrode 16 is adhered, and the active matrix substrate, a twisted nematic (TN) liquid crystal 18 processed by twist orientation is sealed in, and polarizer plates (not shown) are glued to one side each of the two transparent substrates, thereby forming a display device.

As the development of such active matrix substrate becomes intensive, it gives rise to the necessity of forming such active matrix substrate on a large substrate in a range of scores of centimeters at a high yield. At the same time, it is also demanded to fabricate the elements at high density. In fabrication of active matrix substrate, therefore, it is required to process finely and precisely by using exposure machines having the same performance level as that for semiconductor process, and attachments such as the alignment mechanism of high precision. That is, conventionally, to form such an active matrix substrate as shown in FIG. 12, five or six photolithographic processes using photo masks are required.

Such forming method involves several problems as mentioned below in the aspects of cost, yield and performance. First of all, the greater the number of times of photolithography, the more the high performance and expensive exposure machines and others are used, which results in a higher cost for forming the active matrix substrate. Besides, the more the number of times of photolithography, the more troubles may occur in the photolithographic processes (such as misalignment between patterns), and the yield is lowered accordingly. As the substrate material, meanwhile, pyrex and other glass materials are often used, and the strain of the substrate caused by the thermal expansion and contraction during process or stress of the thin film may become too large to be ignored (in particular, this problem is serious in a large substrate, and mismatching between patterns on the substrate formed by photo mask may often exceed 10 microns). As a result, the alignment precision is not uniform within a substrate, and uniformity of the device characteristics decreases, or it may be necessary to use a special apparatus for correcting this strain or to design the device with a special consideration in a margin taking such strain into account. In addition to the substrate strain, the greater the number of times of photo mask matching necessary for realizing the device, the larger becomes the device size for keeping the margin. As a result, the aperture ratio (the rate of effective display region) is lowered. Such phenomena are greater problems when the device density is higher and when the substrate is large. There are also other subjects to be solved, such as

enhancement of the element capacity.

In European patent application 0196915, there is disclosed a self-aligned TFT array for liquid crystal display devices and a method of manufacturing the array. A protective insulating layer on a semiconductor layer is exactly aligned with a gate electrode. A self-alignment method is used for patterning the protective insulating layer and an impurity-doped semiconductor layer on the semiconductor layer. The undoped semiconductor layer itself is patterned by etching, using a separate photomask to pattern a resist film which is then used as a mask for the etching of the semiconductor layer.

In European patent application EP-A-0166647 there is described a method for forming an active matrix substrate, wherein a self-alignment method is used for the positioning of a passivation layer, and by virtue of this for the positioning of the source and drain electrodes.

European patent application EP-A-0222668 discloses a method for forming a thin film transistor in which one semi-conductor layer is formed by a self-alignment process with respect to the gate electrode, in order to simplify the process of producing a stepped semi-conductor layer to which good ohmic contacts can then be made.

It is hence a primary object of this invention, in the light of the above problems, to present a method for fabricating active matrix substrates at a lower cost, by curtailing the photolithographic processes which require precise alignment of photo masks. It is another object of this invention to enhance the performance of the element by employing photolithographic processes which do not require precise alignment of photo masks.

To achieve the above objects, for example, this invention presents a method of fabricating an active matrix substrate, including the steps of:

forming a plurality of gate electrodes of an opaque electro-conducting material by patterning at specified places on a transparent substrate;

forming a gate insulator layer over said gate electrodes;

forming a first semiconductor layer on said gate insulator layer;

forming a second semiconductor layer on said first semiconductor layer;

coating a photoresist layer on the second semiconductor layer;

irradiating light from the back side of the substrate using said gate electrodes as a mask;

forming a resist pattern by developing said photoresist layer;

removing portions of the first and second semiconductor layers which have been irradiated by said light from the backside of the substrate, whereby said first and second semiconductor layers are patterned by a self-alignment process using said gate electrodes as a mask; and

forming a source region and a drain region on said second semiconductor layer by removing portions thereof to expose the first semiconductor layer.

According to the method of this invention, for example, when forming the pattern of semiconductor layer, since photolithography is possible by using the gate electrode (or gate electrode and insular conductor layer) as the mask, an inexpensive exposure machine not requiring the alignment mechanism may be used. Or, depending on the cases, the number of times of photolithography may be curtailed, which contributes to reduction of cost and increase of yield in the production of active matrix substrate. Or when irradiating light from the back side, there is no effect of expansion or contraction of the substrate, and a correctly aligned resist pattern will be obtained. Therefore, by using it, it may be possible to reduce the size of the TFT, and an active matrix substrate of high aperture ratio of high density may be realized. Besides, the device performance may be enhanced, and a high performance inverted staggered type TFT can be realized.

While the novel features of the invention are set forth in the appended claims, the invention, both as to organization and content, will be better understood and appreciated, along with other objects and features thereof, from the following detailed description taken in conjunction with the drawings.

Brief Description of the Drawings

FIG. 1, FIG. 2, FIG. 4B to E, and FIG. 5 to FIG. 13 are process sectional views showing the method for fabricating active matrix substrates in first, second, and fourth to tenth embodiments of the invention, respectively;

FIG. 3 is a sectional view of an active matrix substrate obtained in a third embodiment of the invention;

FIG. 4A is a plan view of an active matrix substrate obtained in a fourth embodiment of the invention;

FIG. 11 is a circuit diagram of an active matrix substrate;

FIG. 12A is a plan view of a thin film transistor for composing a conventional active matrix substrate;

FIG. 12B is a sectional view of line A-B of FIG. 15A; and

FIG. 13 is a sectional view of a conventional display device.

Detailed Description of the Invention

Referring now to the drawings, preferred embodiments of the invention are described in details below.

Example 1

FIG. 1 illustrates a first embodiment of the invention step by step.

On a transparent substrate (for example, Corning Glass 7059) 6, an opaque conductor thin film (for example, Cr; film thickness approx. 100 nm) is deposited by sputtering, and a gate electrode 7 is formed by a desired patterning (FIG. 1A). By plasma enhanced CVD process, a gate insulator layer (first insulator layer, for example, silicon nitride; film thickness approx. 380 nm) 9, a first semiconductor layer (for example, amorphous silicon; film thickness approx. 50 nm) 10, and a passivation layer (for example, silicon nitride; film thickness approx. 80 nm) 11 are sequentially and uniformly deposited, and then the passivation layer 11 is etched, leaving only a part above the gate electrode 7 (FIG. 1B). Next, by plasma enhanced CVD process, again, a second semiconductor layer (for example, phosphorus-doped low resistance amorphous silicon; film thickness approx. 50 nm) 12 is applied, and a positive type photo resist 20 is then coated. After prebaking the resist, ultraviolet ray 21 is irradiated from the back side of the transparent substrate 6, using the gate electrode 7 as the mask (FIG. 1C). When the resist on the substrate is developed, the resist is removed, except for the portion corresponding to the gate electrode 7. After postbaking the resist, using this patterned resist as the etching mask, the exposed areas of the first semiconductor layer 10 and second semiconductor layer 12 are removed by etching (FIG. 1D). After removing the resist, a thin film composed of transparent conductive material (for example, indium tin oxide (ITO); film thickness approx. 400 nm) is deposited, and is patterned, and a drain electrode 13, a source electrode 14, and a pixel electrode 15 are formed (FIG. 1E), so that an active matrix substrate is completed.

As shown in this embodiment, by performing photolithography using the gate electrode 7 as the mask when forming the pattern of semiconductor layer, an inexpensive exposure machine not requiring alignment mechanism can be used, and the number of times of photolithography may be curtailed, too. Besides, since the semiconductor layer is not spreading wider than the gate electrode, the size of the device may be reduced. In this embodiment, meanwhile, the pixel electrode, source electrode and drain electrode are formed simultaneously, but they may be also formed separately.

Example 2

FIG. 2 shows a second embodiment of the invention step by step.

On a light transmissible substrate 6, an opaque conductor thin film is deposited by sputtering, and by patterning as desired a gate electrode 7 and an insular conductor layer 7a are formed (FIG. 2A). By plasma enhanced CVD process, a gate insulator layer (first insulator layer) 9, a first semiconductor layer 10, and a passivation layer 11 are sequentially deposited, and the passivation layer 11 is etched, leaving only a part above the gate electrode 7 (FIG. 2B). Then, after depositing a second semiconductor layer 12 also by plasma enhanced CVD process, a positive type photo resist 20 is coated. After prebaking the resist, ultraviolet ray 21 is irradiated from the back side of the transparent substrate 6, using the gate electrode 7 and insular conductor layer 7a as the mask (FIG. 2C). When the resist on the substrate is developed, the resist is removed except for the portion corresponding to the gate electrode 7 and insular conductor layer 7a. After postbaking the resist, using this resist as the mask the exposed areas of the first semiconductor layer 10 and second semiconductor layer 12 are etched (FIG. 2D). After removing the resist, when a transparent electrode as pixel electrode 15, drain electrode 13, and source electrode 14 are formed (FIG. 2E), an active matrix substrate is completed.

As shown in this embodiment, by forming the semiconductor layer in the great part of the region beneath the source bus line, the redundancy of the source bus line is increased, and disconnection of the source bus line may be prevented.

Example 3

FIG. 3 shows a third embodiment of the invention.

After etching the semiconductor layer in the same manner as in Example 2 (FIG. 2A to D), the resist is removed. Then, a transparent electrode layer is deposited and patterned to form drain electrode 13, source electrode 14 and pixel electrode 15 (FIG. 3), and an active matrix substrate is completed.

Thus, in this embodiment, by forming the pixel electrode, source electrode and drain electrode simultaneously, one step of photolithography can be omitted.

Example 4

FIG. 4 shows a fourth embodiment of the invention.

FIG. 4A is a plan view of essential part of the active matrix array substrate in the fourth embodiment of the invention, showing one pixel and its surrounding parts. Numeral 7 is a gate electrode, 14 is a source electrode, 13 is a drain electrode, and 15 is a pixel electrode. Slits 22 are provided in the gate electrode. FIG. 4B to E are sectional views following step by step along the broken line CD in FIG. 4A. On a transparent substrate, a gate electrode 7 of metal thin film is patterned and formed by using a first photo mask, and a gate insulator layer 9, a first semiconductor layer 10 and a second semiconductor layer 12 are

continuously formed thereon. In this state, a positive type photo resist 20 is coated, and ultraviolet ray 21 is irradiated from the back side of the substrate (FIG. 4B), and the resist on the substrate is developed. At this time, by overexposure, the resist pattern is thinned out by the portion of d1 from the gate electrode 7 (FIG. 4C). Using this resist, furthermore, the first semiconductor layer 10 and second semiconductor layer 12 are etched. At this time, by overetching the etching pattern is thinned out by the portion of d2 from the resist pattern. By the effect of overexposure and overetching (d1+d2), the semiconductor layer is not left over on the gate wiring 7 around the slits 22 (FIG. 4D). By removing the resist, a transparent conductive layer is deposited, and patterning is effected by using a second photo mask, and the source electrode 14, drain electrode 13, and picture element electrode 15 are formed simultaneously. At this time, the second semiconductor layer is etched except for the portion of the second photo mask pattern (FIG. 4E).

In this embodiment, as shown in FIG. 4A, a TFT of which first semiconductor layer 10 is completely separated between adjacent TFTs is completed by using two photo masks.

In the conventional structure, separation of devices (separation of semiconductor layers) was required by some method or other, but when the active matrix array substrate is formed in the method shown herein, a step of photolithography for separation of devices may be saved.

Example 5

FIG. 5 shows a fifth embodiment of the invention.

Same as in Example 1, on a transparent substrate 6, gate electrode 7, gate insulator layer (first insulator layer) 9, first semiconductor layer 10, passivation layer 11, and second semiconductor layer 12 are formed, and a negative type photo resist 23 is coated over the entire surface. After prebaking the resist, an ultraviolet ray 21 is irradiated from the back side of the transparent substrate 6 using the gate electrode 7 as the mask (FIG. 5A to C). When this resist on the substrate is developed, only the resist in the portion corresponding to the gate electrode 7 is removed (FIG. 5D). Next, a conductor layer 24 is deposited (FIG. 5E), and the resist is removed, then the conductor layer 24 except for the portion above the gate electrode 7 is removed together with the resist. Using this conductor layer 24 as the etching mask, the first semiconductor layer 10 and second semiconductor layer 12 are etched (FIG. 5F). Next, a transparent conductive layer is deposited and patterned to form drain electrode 13, source electrode 14 and pixel electrode 15, and then an active matrix substrate is completed (FIG. 5F).

As shown in this embodiment, by performing photolithography using the gate electrode 7 as the mask when forming the pattern of semiconductor layer, an inexpensive exposure machine not requiring alignment mechanism can be used. At the same time, the number of times of photolithography may be curtailed. In this constitution, moreover, part of the source and drain electrodes becomes two-layer, and lowering of resistance of electrode and prevention of disconnection of electrode may be realized.

Example 6

FIG. 6 shows a sixth embodiment of the invention.

Same as in Example 2, on a transparent substrate 6, gate electrode 7, insular conductor layer 7a, gate insulator layer (first insulator layer) 9, first semiconductor layer 10, passivation layer 11, and second semiconductor layer 12 are formed, and a negative type photo resist 23 is coated over the entire surface. After prebaking the resist, ultraviolet ray 21 is irradiated from the back side of the transparent substrate 6 using the gate electrode 7 and insular conductor layer 7a as the mask (FIG. 6A to C). By developing the resist on the substrate, the resist is removed only in the portions corresponding to the gate electrode 7 and insular conductor layer 7a (FIG. 6D). Next, a conductor layer 24 is deposited (FIG. 6E), and the resist is removed, so that the conductor layer 24 is removed together with the resist except for the portion corresponding to the gate electrode 7 and insular conductor layer 7a (FIG. 6F). Using this conductor layer 24 as the etching mask, the first semiconductor layer 10 and second semiconductor layer 12 are patterned, and a transparent conductive layer is deposited and patterned to form drain electrode 13, source electrode 14 and pixel electrode 15, thereby completing an active matrix substrate (FIG. 6G).

Thus, according to this embodiment, by performing photolithography using the gate electrode 7 as the mask when forming patterns of the semiconductor layer, an inexpensive exposure machine not requiring alignment mechanism may be used, and the number of times of photolithography may be curtailed. In addition, by forming the conductor layer 24 and semiconductor layer in the great part of the region beneath the source bus line, the redundancy of the source bus line increases along with lowering of resistance, so that disconnection of the source bus line may be prevented.

Incidentally, as the material of the conductor layer 24 in Examples 5 and 6, Cr, Ta, Ti, Mo, Ni and their alloys, or silicides of these metals may be used.

Example 7

FIG. 7 shows a seventh embodiment of the invention.

Same as in Example 1, on a transparent substrate 6, gate electrode 7, gate insulator layer (first insulator layer) 9, first semiconductor layer 10, passivation layer 11, and second semiconductor layer 12 are formed, and a metal oxide 25 is deposited, and a positive type photo resist 20 is coated over the entire surface. After prebaking the resist, ultraviolet ray 21 is irradiated from the back side of the transparent substrate 6 using the gate electrode 7 as the mask (FIG. 7A to C). When this resist on the substrate is developed, the resist is removed except for the portion corresponding to the gate electrode 7. After postbaking the resist, using this resist as the mask the exposed areas of the metal oxide 25, first semiconductor layer 10 and second semiconductor layer 12 are etched away (FIG. 7D). After removing the resist, when the substrate is exposed to hydrogen plasma atmosphere, the metal oxide 25 is reduced to become a metal layer 14a. Finally, when a transparent electrode as pixel electrode 15, and drain electrode 13 and source electrode 14 are formed (FIG. 7E), an active matrix substrate is completed.

In this embodiment, as shown herein, the performance of the element may be enhanced without increasing the number of steps of photolithography using photo mask. That is, by inserting a metal oxide between the source electrode and drain electrode and the semiconductor layer, and reducing it to a metal, the resistances of the both electrodes may be lowered, and the contact resistance between the source electrode and the semiconductor layer and contact resistance between the drain electrode and the semiconductor layer may be lowered (conventionally, the contact resistance between the second semiconductor layer and the transparent electrode material of the metal oxide was often a problem, and it is improved herein).

Example 8

FIG. 8 shows an eighth embodiment of the invention.

On a transparent substrate 6, a gate electrode 7 and an insular conductor layer 7a are formed, and the rest of the procedure is same as in Example 7, and an active matrix substrate is completed (FIG. 7A to E).

In this embodiment, by forming the semiconductor layer and metal layer in the great part of the region beneath the source bus line, the redundancy of the source bus line is increased, and the disconnection of the source bus line may be prevented. Besides, by the metal layer 14a reduced from the metal oxide, the resistance of the source and drain electrodes is lowered, and the contact resistance between the source electrode and the semiconductor layer and the contact resistance between the drain electrode and the semiconductor layer may be lowered.

In Examples 7, 8, as the metal oxide 25, TaOx and ITO may be adequately used. As the reducing method, instead of the hydrogen plasma processing, other methods such as exposure in hydrogen atmosphere may be equally employed. Anyway, better results are obtained when processed in hydrogen atmosphere or hydrogen plasma atmosphere.

Example 9

FIG. 9 shown a ninth embodiment of the invention.

Same as in Example 1, on a transparent substrate 6, gate electrode 7, gate insulator layer (first insulator layer) 9, first semiconductor layer 10, passivation layer 11, and second semiconductor layer 12 are formed, and a positive type photo resist 20 is coated, and ultraviolet ray 21 is irradiated from the back side of the transparent substrate 6 using the gate electrode 7 as mask (FIG. 9A to C). After developing this resist, the exposed areas of the first semiconductor layer 10, and second semiconductor layer 12 are etched. Next, a metal oxide film composed of at least one layer of metal oxide film, for example, 90% In_2O_3 - 10% SnO_2 is deposited, and patterned to form drain electrode 13, source electrode 14, and pixel electrode 15 (FIG. 9D). On this, a negative type photo resist 23 is coated, and ultraviolet ray is irradiated from the back side of the transparent substrate 6 using the gate electrode 7 as mask. After developing the resist (FIG. 9E), the substrate is exposed in hydrogen plasma atmosphere, and part of the drain electrode 13 and source electrode 14 is reduced to become In-Sn. When the resist is removed, an active matrix substrate is completed (FIG. 9F).

Thus, in this embodiment, by reducing the source electrode and drain electrode to transform into metals, the both electrodes may be lowered in resistance, and the contact resistance between the source electrode and semiconductor layer and the contact resistance between the drain electrode and semiconductor layer may be lowered.

Example 10

FIG. 10 shows a tenth embodiment of the invention.

Same as in Example 1, on a tranparent substrate 6, gate electrode 7, gate insulator layer (first insulator layer) 9, first semiconductor layer 10, passivation layer 11 and second semiconductor layer 12 are formed, and a positive type photo resist 20 is coated, and ultraviolet ray 21 is irradiated from the back side of the transparent substrate 6 using the gate electrode 7 as mask (FIG. 10A). After developing this resist, exposed areas of the first semiconductor layer 10 and second semiconductor layer 12 are etched. A two-layer metal oxide film composed of at least one metal oxide film such as 90% In_2O_3-10% SnO_2, and Ta_2O_5 is

deposited (the side contacting with the semiconductor is 90% In_2O_3-10% SnO_2), and patterned, and drain electrode 13, source electrode 14 and pixel electrode 15 are formed, and a second insulator layer 19 is deposited thereon (FIG. 10B). On this, furthermore, a negative type photo resist 23 is coated, and ultraviolet ray is irradiated from the back side of the transparent substrate 6 using the gate electrode 7 as mask. By developing the resist, the portion not covered by the resist of the second insulator layer 19 is etched (FIG. 10C), and the substrate is exposed to hydrogen plasma atmosphere, then the metal oxide films of the drain electrode 13 and source electrode 14 are reduced to form a two-layer metal film composed of In-Sn and Ta. At this time, when the active matrix substrate is exposed in an oxygen plasma atmosphere or oxidized anodically, the surface layer of the reduced drain electrode 13 and source electrode 14 are oxidized again to be insulation layer, and when the resist is removed, an active matrix substrate is completed (FIG. 10D).

In this embodiment, thus, by reducing the source electrode and drain electrode to transform into metals, the both electrodes are lowered in resistance, while the contact resistance between the source electrode and semiconductor layer and the contact resistance between the drain electrode and semiconductor layer are lowered at the same time. Besides, by oxidizing the surface, the insulation layers of the both electrode surfaces and the second insulator layer 19 become passivation of active matrix substrate.

In Examples 9, 10, meanwhile, as the materials for drain electrode, source electrode and pixel electrode, 90% In_2O_3-10% SnO_2 or 90% In_2O_3-10% SnO_2, and TaO_5 are used, but other materials which show conductivity when reduced may be similarly applied. Anyway, better results will be obtained when one or more metal oxides selected from a group consisting of In, Sn, Cd, Zn, Nb, Ti and Ta are employed.

Besides, in Examples 9, 10, are the drain electrode and source electrode are reduced by processing in hydrogen plasma, but it may be also possible to reduced by exposing to hydrogen atmosphere or the like. However, the best results will be obtained by hydrogen plasma processing.

In the above embodiments from Example 1 to Example 10, as the gate electrode material, Cr, Ta, Ti, Mo, Ni, Ni-Cr or their metal silicides may be used. Any opaque conductive material may be employed as far as it may be used as the material for the gate electrode of the TFT. As the materials for the gate insulator layer and passivation layer, aside from silicon nitride, silicon oxide, metal oxide and other transparent insulators may be used. As the first and second semiconductor layers, amorphous silicon or phosphorus-doped amorphous silicon was used, but any semiconductor material may be equally used as far as it can obtain required TFT characteristics and pass ultraviolet rays to a certain extent, and, for example, polycrystal silicon or recrystallized silicon may be used. Furthermore, as the material for the pixel electrode, InOx, SnOx or transparent conductive material (ITO) of their mixed composition may be used. When forming, meanwhile, the source electrode, drain electrode and picture element electrode separately, various conductive materials (Al, Mo, Ni, other metals or their silicides) may be used as the materials for source electrode and drain electrode. In this case, the source and drain electrodes may be formed either in a single layer or in plural layers.

Besides, before coating the positive or negative type photo resist, by using a primer for the resist, the adhesion of the resist will be enhanced.

As clear from the embodiments illustrated and described herein, according to the method for fabricating the active matrix substrate of the invention, an inexpensive exposure machine not requiring alignment mechanism may be used, and the photolithographic process requiring the photo mask may be curtailed, so that the reduction of cost which is the greatest subject in the active matrix type liquid crystal display device may be realized. Besides, the performance of the element may be improved by employing the photolithographic process which does not require precise alignment of mask. Therefore, its industrial significance is extremely great.

Claims

1. A method of fabricating an active matrix substrate, including the steps of:

   forming a plurality of gate electrodes (7) of an opaque electro-conducting material by patterning at specified places on a transparent substrate (6);

   forming a gate insulator layer (9) over said gate electrodes (7);

   forming a first semiconductor layer (10) on said gate insulator layer (9);

   forming a second semiconductor layer (12) on said first semiconductor layer (10);

   coating a photoresist layer (20, 23) on the second semiconductor layer;

   irradiating light from the back side of the substrate (6) using said gate electrodes (7) as a mask;

   forming a resist pattern by developing said photoresist layer (20, 23);

   removing portions of the first and second semiconductor layers (10, 12) which have been irradiated by said light from the backside of the substrate (6), whereby said first and second semiconductor layers (10, 12) are patterned by a self-alignment process using said gate electrodes (7) as a mask; and

forming a source region and a drain region on said second semiconductor layer (12) by removing portions thereof to expose the first semiconductor layer (10).

2. A method of fabricating an active matrix substrate according to claim 1, further comprising steps of

forming a passivation layer (11) by patterning on said first semiconductor layer (10) above a part of each gate electrode (7); and

forming a drain electrode (13), a source electrode (14) and a pixel electrode (15) by depositing a layer of transparent conductive material on each said drain and said source region and patterning it.

3. A method of fabricating an active matrix substrate according to claim 1, further comprising a step of

forming an insular region (7a) of the same opaque electro-conducting material as said gate electrodes (7) by patterning at a specified place of the transparent substrate (6), wherein said first and second semiconductor layers (10, 12) are formed above said insular region (7a) by the self alignment process using said insular region (7a) as the mask.

4. A method of fabricating an active matrix substrate according to claim 3, further comprising a step of

forming a drain electrode (13), a source electrode (14) and a pixel electrode (15) by depositing a layer of transparent conductive material on each said drain and said source region and patterning it.

5. A method of fabricating an active matrix substrate according to claim 1, further comprising the steps of

forming slits (22) in selected gate electrodes (7), wherein in said steps of irradiating and forming a resist pattern, said photoresist layer (20) is overexposed and over-etched such as to allow removal of the semiconductor layers (10, 12) from around the slits (22) in said selected gate electrodes (7); and

forming a drain electrode (13), a source electrode (14) and a pixel electrode (15) by depositing a layer of transparent conductive material on each said drain and said source region and patterning it.

6. A method of fabricating an active matrix substrate according to claim 1, further comprising the steps of

forming a passivation layer (11) by patterning on said first semiconductor layer (10) above a part of said gate electrodes (7);

forming a conductor layer (24) on the portion of the semiconductor layer (12) above said gate electrodes (7) prior to the step of forming said source and drain regions; wherein said step further comprises removing portions of said conductor layer (24) as well as portions of said semiconductor layer (12) from above said gate electrode layer (7) to expose the first semiconductor layer (10); and

forming a drain electrode (13), a source electrode (14) and a pixel electrode (15) by depositing and patterning a layer of transparent conductive material on the remaining portions of the conductor layer (24).

7. A method of fabricating an active matrix substrate according to claim 6, further comprising the steps of

forming an insular region (7a) of the same opaque electro-conducting material as said gate electrodes (7) by patterning at a specified place of the transparent substrate (6), wherein said first and second semiconductor layers (10, 12) and said conductor layer (24) are formed above said insular region (7a) by the self-alignment process using said insular layer (7a) as the mask.

8. A method of fabricating an active matrix substrate according to claim 1, further comprising a step of

forming a passivation layer (11) by patterning on said first semiconductor layer (10) above a part of said gate electrodes (7);

depositing a metal oxide layer (25) on said second semiconductor layer (12) prior to said step of coating a photoresist layer (25) thereon, such that said metal oxide layer (25) is also patterned by the self-alignment process using the gate electrodes (7) as the mask, wherein the step of forming the source and drain regions further comprises removing portions of the metal oxide layer (25) as well as portions of said second semiconductor layer (12) from above said gate electrode (7) to expose the first semiconductor layer (10);

reducing the metal oxide layer (25) to produce a metal layer (14a); and

forming a drain electrode (13), a source electrode (14) and a pixel electrode (15) by depositing and patterning a layer of transparent conductive material on the remaining portions of the metal layer (14a).

9. A method of fabricating an active matrix substrate according to claim 8, further comprising steps of

forming an insular region (7a) of the same opaque electro-conducting material as said gate electrodes (7) by patterning at a specified place of the transparent substrate (6), wherein said first and second semiconductor layers (10, 12) and said metal layer (14a) are formed above said insular region (7a) using said insular region (7a) as the mask.

10. A method of fabricating an active matrix substrate according to claim 1, further comprising the steps of

depositing a metal oxide layer on said second semiconductor layer (12) after the step of forming the source and drain regions;

patterning said metal oxide layer to form a drain electrode (13), a source electrode (14) and a pixel electrode (15);

coating a negative type photoresist (23) on said metal oxide layer;

irradiating light from the back side of the substrate (6);

developing the resist (23); and

reducing the exposed part of the source electrode (14) and the drain electrode (13).

11. A method of fabricating an active matrix substrate according to claim 1, further comprising the steps of

depositing a two-layer metal oxide film comprising at least one metal oxide layer on said second semiconductor layer (12) after the step of forming the source and drain regions;

patterning said metal oxide film to form a drain electrode (13), a source electrode (14) and a pixel electrode (15);

depositing a second insulator layer (19) thereon;

coating a negative type photoresist (23) on said second insulator layer (19);

irradiating light from the back side of the substrate (6) using the gate electrodes (7) as the mask;

developing the resist (23);

removing the exposed part of the second insulating layer (19) not covered by the resist (23);

reducing the metal oxide films of the drain electrode (13) and source electrode (14) to form a two-layer metal film;

oxidizing the surface layer of the drain electrode (13) and the source electrode (14); and

removing the remaining portions of the resist (23).

Patentansprüche

1. Ein Verfahren zum Herstellen eines aktiven Matrixsubstrats mit den folgenden Schritten:
Bilden einer Vielzahl von Gate-Elektroden (7) aus einem lichtundurchlässigen elektroleitfähigen Material durch Strukturierung an bestimmten Stellen auf einem transparenten Substrat (6);
Bilden einer Gate-Isolationsschicht (9) über den Gate-Elektroden (7);
Bilden einer ersten Halbleiterschicht (10) auf der Gate-Isolationsschicht (9);
Bilden einer zweiten Halbleiterschicht (12) auf der ersten Halbleiterschicht (10);
Aufbringen einer Fotoresistschicht (20, 23) auf die zweite Halbleiterschicht;
Einstrahlen von Licht von der Rückseite des Substrats (6) unter Verwendung der Gate-Elektroden (7) als Maske;
Bilden eines Resistmusters durch Entwickeln der Fotoresistschicht (20, 23);
Entfernen von Abschnitten der ersten und zweiten Halbleiterschichten (10, 12), die durch das Licht von der Rückseite des Substrats (6) bestrahlt worden sind, wobei die erste und zweite Halbleiterschicht (10, 12) durch ein Selbstausrichtverfahren unter Verwendung der Gate-Elektroden (7) als Maske strukturiert werden; und
Bilden eines Source-Bereichs und eines Drain-Bereichs auf der zweiten Halbleiterschicht (12) durch Entfernen von Teilen davon, um die erste Halbleiterschicht (10) freizulegen.

2. Ein Verfahren zum Herstellen eines aktiven Matrixsubstrats gemäß Anspruch 1, das weiter die Schritte umfaßt:
Bilden einer Passivierungsschicht (11) durch Strukturierung auf der ersten Halbleiterschicht (10) über einem Teil jeder Gate-Elektrode (7); und
Bilden einer Drain-Elektrode (13), einer Source-Elektrode (14) und einer Bildpunktelektrode (15) durch Ablagern und Strukturieren einer Schicht aus transparentem, leitfähigem Material auf jedem der Drain- und Source-Bereiche.

3. Ein Verfahren zum Herstellen eines aktiven Matrixsubstrats gemäß Anspruch 1, das weiter einen Schritt umfaßt
des Bilden eines inselartigen Bereichs (7a) aus dem gleichen lichtundurchlässigen elektroleitfähigen Material wie die Gate-Elektroden (7) durch Strukturierung an einer bestimmten Stelle auf dem transparenten Substrat (6), wobei die ersten und zweiten Halbleiterschichten (10, 12) über dem inselartigen Bereich (7a) durch das Selbstausrichtverfahren unter Verwendung des insel-

artigen Bereichs (7a) als Maske gebildet werden.

4. Ein Verfahren zum Herstellen eines aktiven Matrixsubstrats gemäß Anspruch 3, das weiter einen Schritt umfaßt
des Bildens einer Drain-Elektrode (13), einer Source-Elektrode (14) und einer Bildpunktelektrode (15) durch Ablagern und Strukturieren einer Schicht aus transparentem, leitfähigem Material auf jedem der Drain- und Source-Bereiche.

5. Ein Verfahren zum Herstellen eines aktiven Matrixsubstrats gemäß Anspruch 1, das weiter die folgenden Schritte umfaßt:
Bilden von Schlitzen (22) in ausgewählten Gate-Elektroden (7), wobei bei den Schritten des Bestrahlens und Bildens eines Resistmusters die Fotoresistschicht (20) überbelichtet und überätzt wird, um somit eine Abtragung der Halbleiterschichten (10, 12) um die Schlitze (22) herum in den ausgewählten Gate-Elektroden (7) zu ermöglichen; und
Bilden einer Drain-Elektrode (13), einer Source-Elektrode (14) und einer Bildpunktelektrode (15) durch Ablagern und Strukturieren einer Schicht aus transparentem, leitfähigem Material auf jedem der Source- und Drain-Bereiche.

6. Ein Verfahren zum Herstellen eines aktiven Matrixsubstrats gemäß Anspruch 1, das weiter die Schritte umfaßt:
Bilden einer Passivierungsschicht (11) durch Strukturierung auf der ersten Halbleiterschicht (10) über einem Teil der Gate-Elektroden (7);
Bilden einer Leiterschicht (24) auf dem Abschnitt der Halbleiterschicht (12) über den Gate-Elektroden (7) vor dem Schritt des Bildens der Source- und Drain-Bereiche; wobei der Schritt weiter ein Entfernen von Teilen der Leiterschicht (24) wie auch von Teilen der Halbleiterschicht (12) über der Gate-Elektrodenschicht (7) umfaßt, um die erste Halbleiterschicht (10) freizulegen; und
Bilden einer Drain-Elektrode (13), einer Source-Elektrode (14) und einer Bildpunktelektrode (15) durch Ablagern und Strukturieren einer Schicht aus transparentem, leitfähigem Material auf den verbleibenden Abschnitten der Leiterschicht (24).

7. Ein Verfahren zum Herstellen eines aktiven Matrixsubstrats gemäß Anspruch 6, das weiter den Schritt umfaßt
des Bildens eines inselartigen Bereichs (7a) aus dem gleichen lichtundurchlässigen, elektroleitfähigen Material wie die Gate-Elektroden (7) durch Strukturieren an einer bestimmten Stelle auf dem transparenten Substrat (6), wobei die erste und zweite Halbleiterschicht (10, 12) und die Leiterschicht (24) über dem inselartigen Bereich (7a) durch das Selbstausrichtverfahren unter Verwendung der inselartigen Schicht (7a) als Maske geformt werden.

8. Ein Verfahren zum Herstellen eines aktiven Matrixsubstrats gemäß Anspruch 1, das weiter die Schritte umfaßt
des Bildens einer Passivierungsschicht (11) durch Strukturierung auf der ersten Halbleiterschicht (10) über einem Teil der Gate-Elektroden (7);
des Ablagerns einer Metalloxidschicht (25) auf der zweiten Halbleiterschicht (12) vor dem Schritt des Aufbringens einer Fotoresistschicht (25) auf diese, so daß die Metalloxidschicht (25) ebenfalls durch das Selbstausrichtverfahren unter Verwendung der Gate-Elektroden (7) als Maske strukturiert wird, wobei der Schritt des Bildens der Source- und DrainBereiche weiter eine Entfernung von Teilen der Metalloxidschicht (25) wie auch von Teilen der zweiten Halbleiterschicht (12) über der Gate-Elektrode (7) umfaßt, um die erste Halbleiterschicht (10) freizulegen;
des Reduzierens der Metalloxidschicht (25) zur Erzeugung einer Metallschicht (14a); und
des Bildens einer Drain-Elektrode (13), einer Source-Elektrode (14) und einer Bildpunktelektrode (15) durch Ablagerung und Strukturierung einer Schicht aus transparentem, leitfähigem Material auf den verbleibenden Abschnitten der Metallschicht (14a).

9. Ein Verfahren zum Herstellen eines aktiven Matrixsubstrats gemäß Anspruch 8, das den weiteren Schritt umfaßt
des Bildens eines inselartigen Bereichs (7a) aus dem gleichen lichtundurchlässigen, elektroleitfähigen Material wie die Gate-Elektroden (7) durch Strukturierung an einer bestimmten Stelle auf dem transparenten Substrat (6), wobei die erste und zweite Halbleiterschicht (10, 12) und die Metallschicht (14a) über dem inselartigen Bereich (7a) unter Verwendung des inselartigen Bereichs (7a) als Maske gebildet werden.

10. Ein Verfahren zum Herstellen eines aktiven Matrixsubstrats gemäß Anspruch 1, das weiter die Schritte umfaßt
des Ablagerns einer Metalloxidschicht auf der zweiten Halbleiterschicht (12) nach dem Schritt des Bildens der Source- und Drain-Bereiche;
des Strukturierens der Metalloxidschicht zur Bildung einer Drain-Elektrode (13), einer Source-Elektrode (14) und einer Bildpunktelektrode (15);
des Aufbringens eines Fotoresists (23) eines negativen Typs auf die Metalloxidschicht;
des Einstrahlens von Licht von der Rückseite des

Substrats (6);
des Entwickelns des Resits (23); und
des Reduzierens des freiliegenden Teils der Source-Elektrode (14) und der Drain-Elektrode (13).

11. Ein Verfahren zum Herstellen eines aktiven Matrixsubstrats gemäß Anspruch 1, das weiter die Schritte umfaßt
des Ablagerns eines zweischichtigen Metalloxidfilms mit wenigstens einer Metalloxidschicht auf der zweiten Halbleiterschicht (12) nach dem Schritt des Bildens der Source- und Drain-Bereiche;
des Strukturierens des Metalloxidfilms zur Bildung einer Drain-Elektrode (13), einer Source-Elektrode (14) und einer Bildpunktelektrode (15);
des Ablagerns einer zweiten Isolationsschicht (19) darauf;
des Aufbringens eines Fotoresists (23) eines negativen Typs auf die zweite Isolationsschicht (19);
des Einstrahlens von Licht von der Rückseite des Substrats (6) unter Verwendung der Gate-Elektroden (7) als Maske;
des Entwickelns des Resists (23);
des Entfernens des freiliegenden Teils der zweiten Isolationsschicht (19), die nicht durch den Fotoresist (23) abgedeckt ist;
des Reduzierens des Metalloxidfilms der Drain-Elektrode (13) und der Source-Elektrode (14) zur Bildung eines zweischichtigen Metallfilms;
des Oxidierens der Oberflächenschicht der Drain-Elektrode (13) und der Source-Elektrode (14); und
des Entfernens des verbleibenden Abschnitts des Resists (23).

Revendications

1. Procédé de fabrication d'un substrat à matrice active incluant les étapes de :
formation d'une pluralité d'électrodes de grille (7) en un matériau électroconducteur opaque au moyen d'une conformation en des endroits spécifiés sur un substrat transparent (6) ;
formation d'une couche d'isolation de grille (9) sur lesdites électrodes de grille (7) ;
formation d'une première couche semiconductrice (10) sur ladite couche d'isolation de grille (9) ;
formation d'une seconde couche semiconductrice (12) sur ladite première couche semiconductrice (10) ;
dépôt d'une couche de photoréserve (20, 23) sur la seconde couche semiconductrice ;
irradiation d'une lumière depuis le côté arrière du substrat (6) en utilisant lesdites électrodes de grille (7) en tant que masque ;
formation d'un motif de réserve en développant ladite couche de photoréserve (20, 23) ;
enlèvement de parties des première et seconde couches semiconductrices (10, 12) qui ont été irradiées par ladite lumière provenant du côté arrière du substrat (6) de telle sorte que lesdites première et seconde couches semiconductrices (10) soient conformées au moyen d'un processus d'auto-alignement en utilisant lesdites électrodes de grille (7) en tant que masque ; et
formation d'une région de source et d'une région de drain sur ladite seconde couche semiconductrice (12) en ôtant certaines de ses parties afin de mettre à nu la première couche semiconductrice (10).

2. Procédé de fabrication d'un substrat à matrice active selon la revendication 1, comprenant en outre les étapes de :
formation d'une couche de passivation (11) au moyen d'une conformation sur ladite première couche semiconductrice (10) au-dessus d'une partie de chaque électrode de grille (7) ; et
formation d'une électrode de drain (13), d'une électrode de source (14) et d'une électrode de pixel (15) en déposant une couche en un matériau conducteur transparent sur chaque dite région prise parmi ladite région de source et ladite région de drain et en la conformant.

3. Procédé de fabrication d'un substrat à matrice active selon la revendication 1, comprenant en outre les étapes de :
formation d'une région insulaire (7a) en le même matériau électroconducteur opaque que lesdites électrodes de grille (7) au moyen d'une conformation en un endroit spécifié du substrat transparent (6), lesdites première et seconde couches semiconductrices (10, 12) étant formées au-dessus de ladite région insulaire (7a) par le processus d'auto-alignement en utilisant ladite région insulaire (7a) en tant que masque.

4. Procédé de fabrication d'un substrat à matrice active selon la revendication 3, comprenant en outre l'étape de :
formation d'une électrode de drain (13), d'une électrode de source (14) et d'une électrode de pixel (15) en déposant une couche en un matériau conducteur transparent sur chaque région prise parmi ladite région de drain et ladite région de source et en la conformant.

5. Procédé de fabrication d'un substrat à matrice active selon la revendication 1, comprenant en outre les étapes de :

formation de fentes (22) dans des électrodes de grille sélectionnées (7), dans lequel, lors desdites étapes d'irradiation et de formation d'un motif de réserve, ladite couche de photoréserve (20) est sur-mise à nu et sur-gravée de manière à permettre l'enlèvement des couches semiconductrices (10, 12) d'autour des fentes (22) ménagées dans lesdites électrodes de grille sélectionnées (7) ; et

formation d'une électrode de drain (13), d'une électrode de source (14) et d'une électrode de pixel (15) en déposant une couche en un matériau conducteur transparent sur chaque région prise parmi ladite région de drain et ladite région de source et en la conformant.

6. Procédé de fabrication d'un substrat à matrice active selon la revendication 1, comprenant en outre les étapes de :

formation d'une couche de passivation (11) au moyen d'une conformation sur ladite première couche semiconductrice (10) au-dessus d'une partie desdites électrodes de grille (7) ;

formation d'une couche conductrice (24) sur la partie de la couche semiconductrice (12) au-dessus desdites électrodes de grille (7) avant l'étape de formation desdites régions de source et de drain ; dans lequel ladite étape comprend en outre l'enlèvement de parties de ladite couche conductrice (24) ainsi que de parties de ladite couche semiconductrice (12) du dessus de ladite couche d'électrode de grille (7) afin de mettre à nu la première couche semiconductrice (10) ; et

formation d'une électrode de drain (13), d'une électrode de source (14) et d'une électrode de pixel (15) en déposant et en conformant une couche en un matériau conducteur transparent sur les parties restantes de la couche conductrice (24).

7. Procédé de fabrication d'un substrat à matrice active selon la revendication 6, comprenant en outre les étapes de :

formation d'une région insulaire (7a) en le même matériau électroconducteur opaque que lesdites électrodes de grille (7) en réalisant une conformation en un endroit spécifié du substrat transparent (6), lesdites première et seconde couches semiconductrices (10, 12) et ladite couche conductrice (24) étant formées au-dessus de ladite région insulaire (7a) au moyen du processus d'auto-alignement en utilisant ladite couche insulaire (7a) en tant que masque.

8. Procédé de fabrication d'un substrat à matrice active selon la revendication 1, comprenant en outre les étapes de :

formation d'une couche de passivation (11) en réalisant une conformation sur ladite première couche semiconductrice (10) au-dessus d'une partie desdites électrodes de grille (7) ;

dépôt d'une couche d'oxyde métallique (25) sur ladite seconde couche semiconductrice (12) avant ladite étape de dépôt d'une couche de photoréserve (25) dessus de telle sorte que ladite couche d'oxyde métallique (25) soit également conformée par le processus d'auto-alignement en utilisant les électrodes de grille (7) en tant que masque, dans lequel l'étape de formation des régions de source et de drain comprend en outre l'enlèvement de parties de la couche d'oxyde métallique (25) ainsi que de parties de ladite seconde couche semiconductrice (12) du dessus de ladite électrode de grille (7) afin de mettre à nu la première couche semiconductrice (10) ;

réduction de la couche d'oxyde métallique (25) pour produire une couche de métal (14a) ; et

formation d'une électrode de drain (13), d'une électrode de source (14) et d'une électrode de pixel (15) en déposant et en conformant une couche en un matériau conducteur transparent sur les parties restantes de la couche de métal (14a).

9. Procédé de fabrication d'un substrat à matrice active selon la revendication 8, comprenant en outre les étapes de :

formation d'une région insulaire (7a) en le même matériau électroconducteur opaque que lesdites électrodes de grille (7) en réalisant une conformation en un endroit spécifié du substrat transparent (6), lesdites première et seconde couches semiconductrices (10, 12) et ladite couche de métal (14a) étant formées au-dessus de ladite région insulaire (7a) en utilisant ladite région insulaire (7a) en tant que masque.

10. Procédé de fabrication d'un substrat à matrice active selon la revendication 1, comprenant en outre les étapes de :

dépôt d'une couche d'oxyde métallique sur ladite seconde couche semiconductrice (12) après l'étape de formation des régions de source et de drain ;

conformation de ladite couche d'oxyde métallique pour former une électrode de drain (13), une électrode de source (14) et une électrode de pixel (15) ;

dépôt d'une photoréserve du type négatif (23) sur ladite couche d'oxyde métallique ;

irradiation d'une lumière depuis le côté arrière du substrat (6) ;

développement de la réserve (23) ; et

réduction de la partie mise à nu de l'électrode de source (14) et de l'électrode de drain (13).

11. Procédé de fabrication d'un substrat à matrice active selon la revendication 1, comprenant en outre les étapes de :

dépôt d'un film d'oxyde métallique bicouche comprenant au moins une couche d'oxyde métallique sur ladite seconde couche semiconductrice (12) après l'étape de formation des réglons de source et de drain ;

conformation dudit film d'oxyde métallique pour former une électrode de drain (13), une électrode de source (14) et une électrode de pixel (15) ;

dépôt d'une seconde couche isolante (19) dessus ;

dépôt d'une photoréserve du type négatif (23) sur ladite seconde couche isolante (19) ;

irradiation d'une lumière depuis le côté arrière du substrat (6) en utilisant les électrodes de grille (7) en tant que masque ;

développement de la réserve (23) ;

enlèvement de la partie mise à nu de la seconde couche isolante (19) non recouverte par la réserve (23) ;

réduction des films d'oxyde métallique de l'électrode de drain (13) et de l'électrode de source (14) pour former un film métallique bicouche ;

oxydation de la couche de surface de l'électrode de drain (13) et de l'électrode de source (14) ; et

enlèvement des parties restantes de la réserve (23).

Fig. 1A

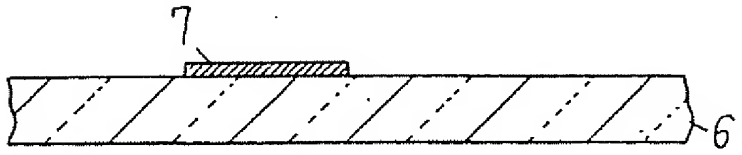


Fig. 1B

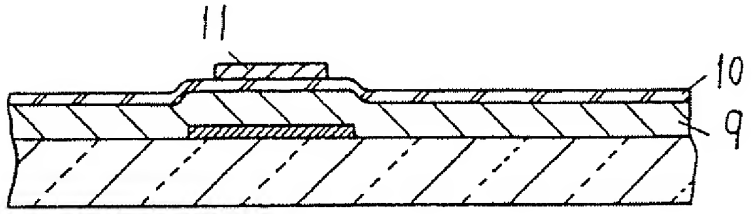


Fig. 1C

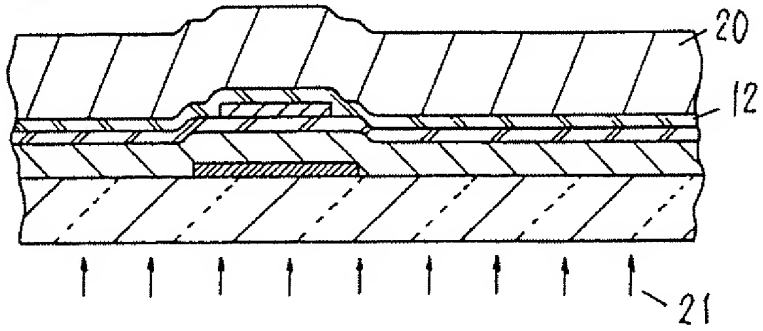


Fig. 1D

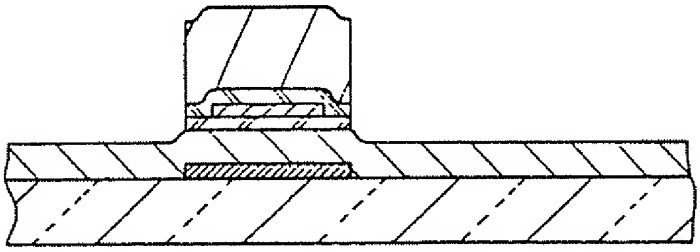


Fig. 1E

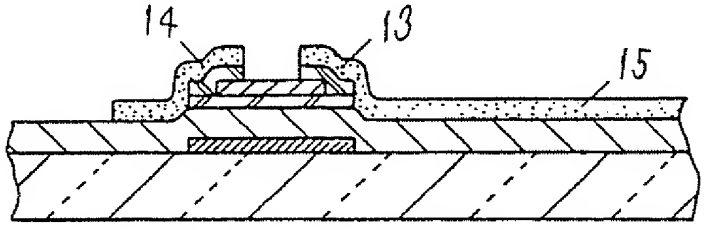


Fig. 2 A

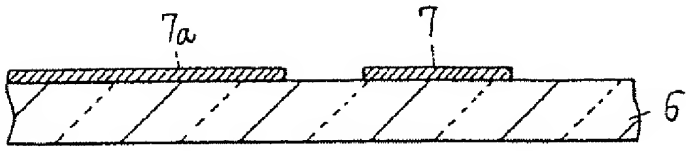


Fig. 2 B

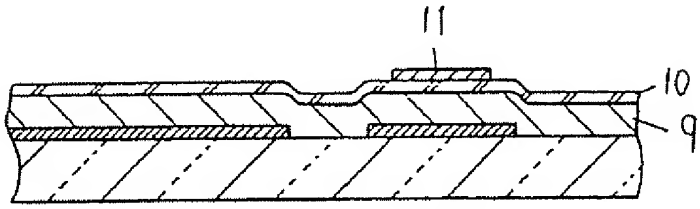


Fig. 2 C

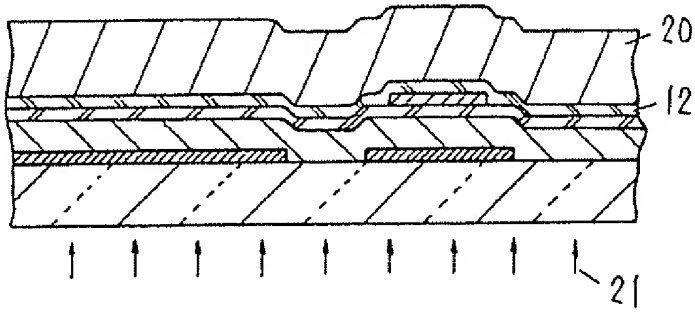


Fig. 2 D

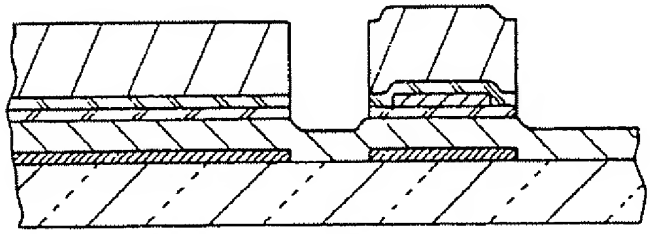


Fig. 2 E

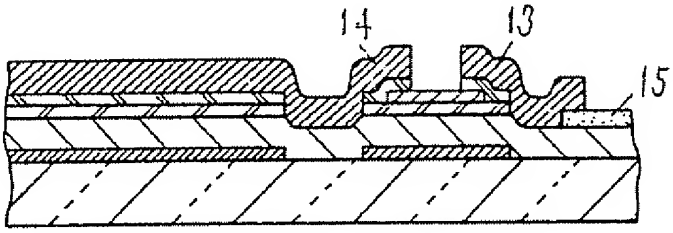


Fig. 3

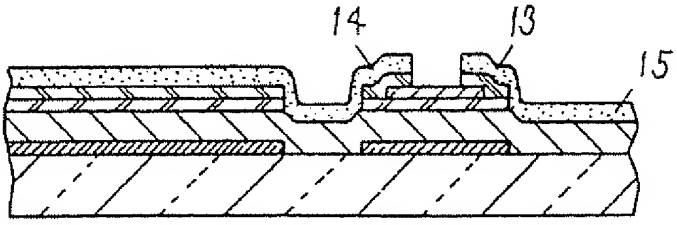


Fig.4 A

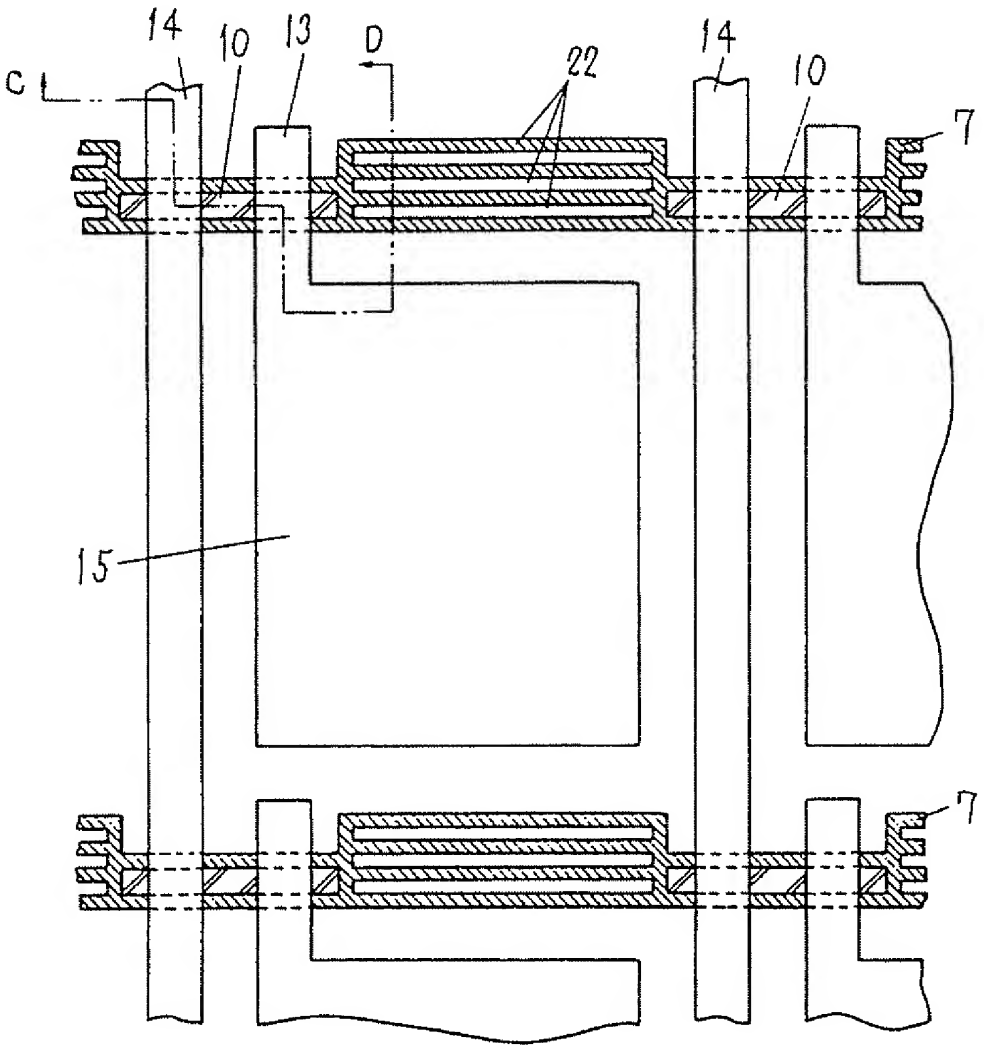


Fig.4 B

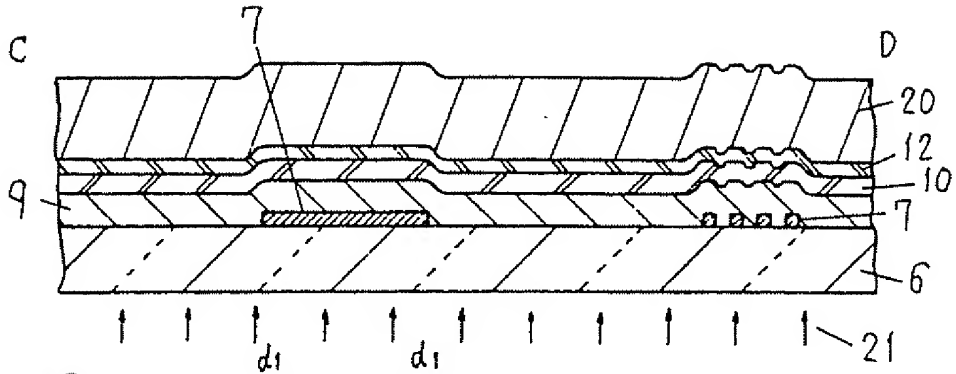


Fig.4C

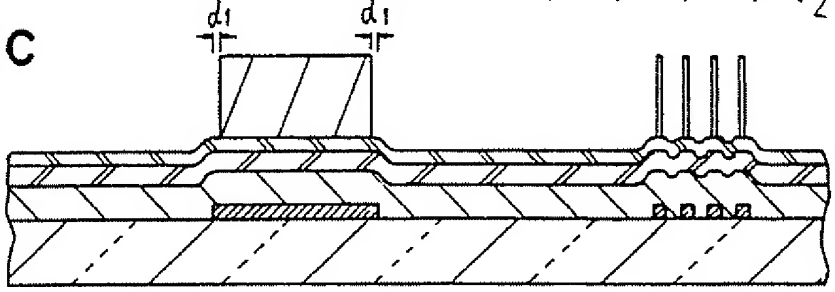


Fig.4D

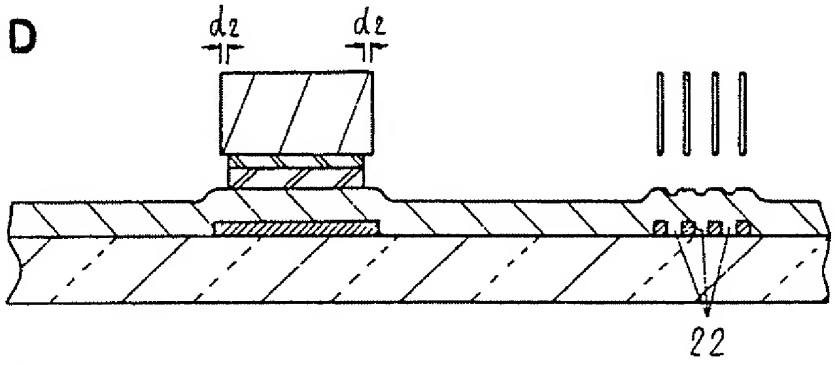


Fig.4E

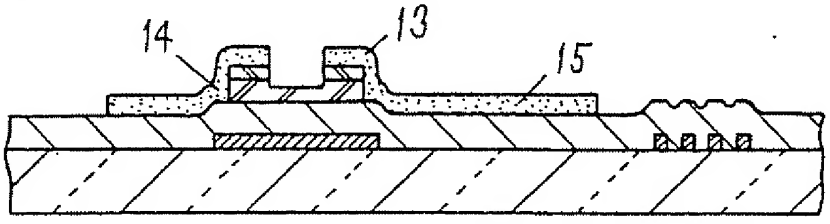


Fig.5A

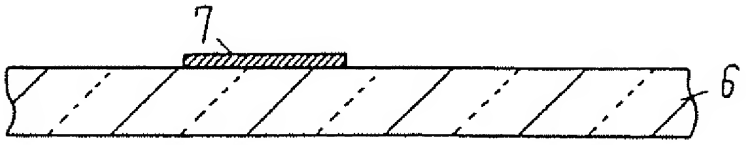


Fig.5B

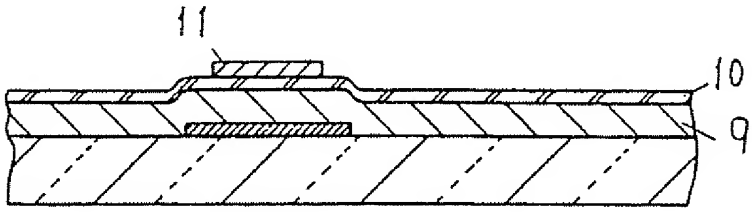


Fig.5C

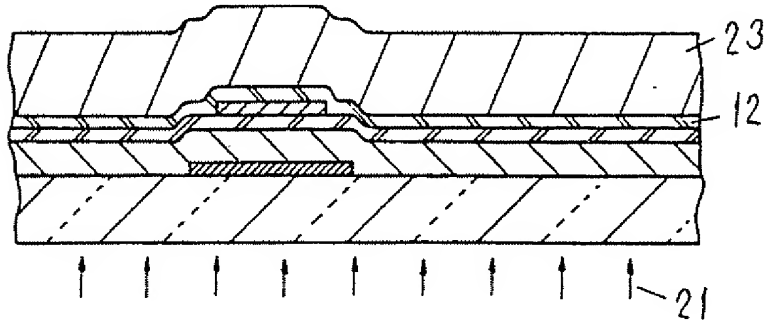


Fig.5D

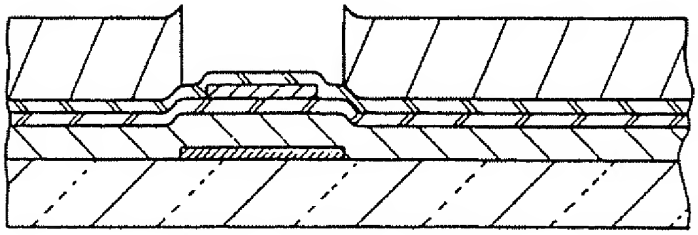


Fig.5E

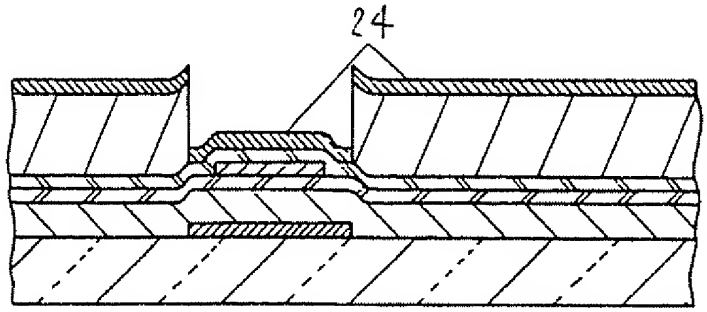


Fig.5 F

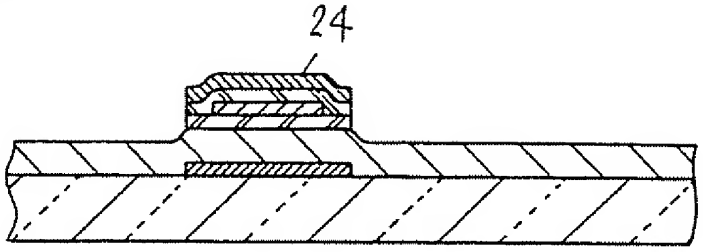


Fig.5 G

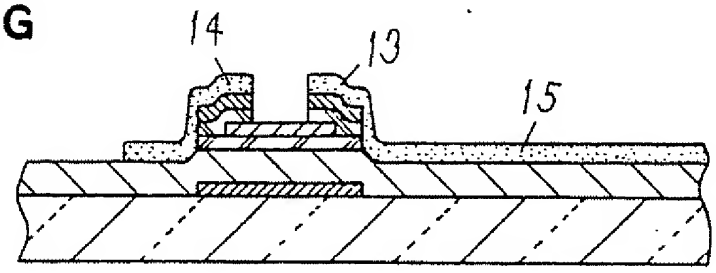


Fig.6 A

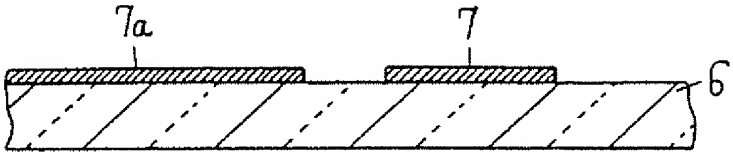


Fig.6 B

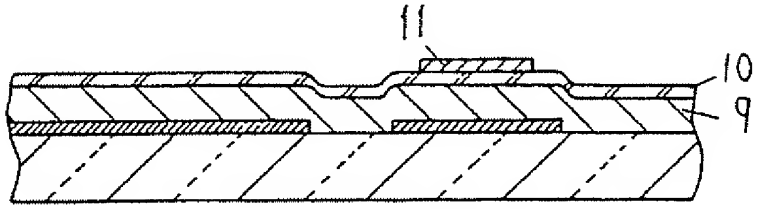


Fig.6 C

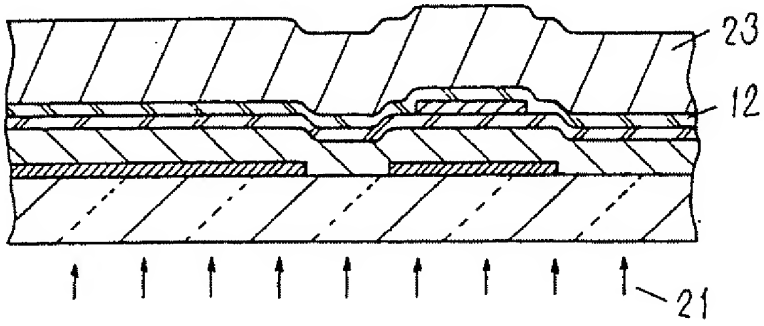


Fig.6 D

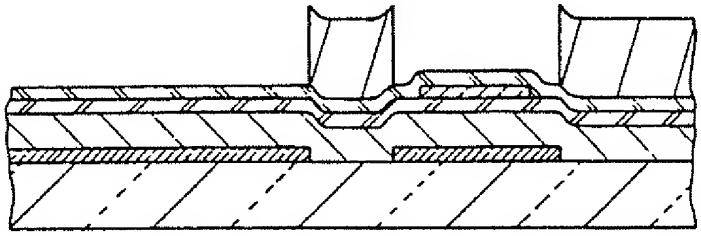


Fig.6 E

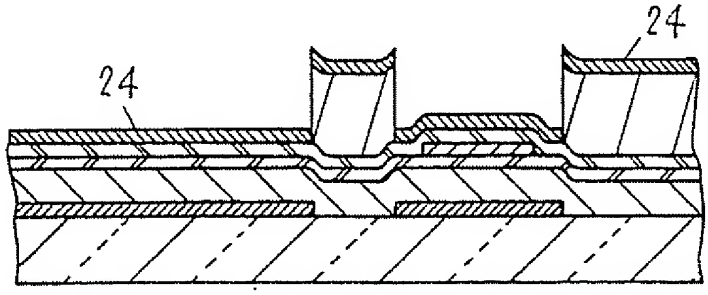


Fig.6 F

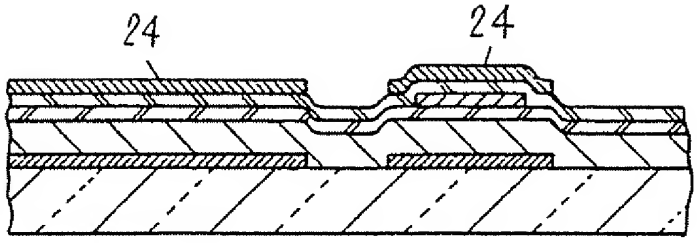


Fig.6 G

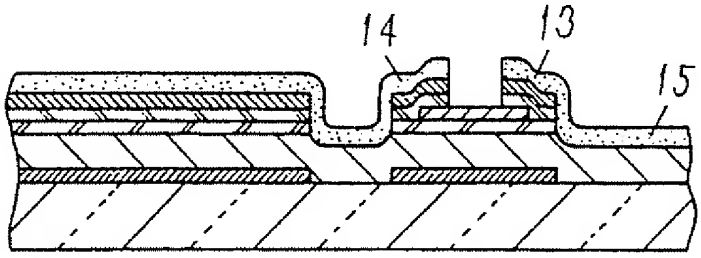


Fig.7A

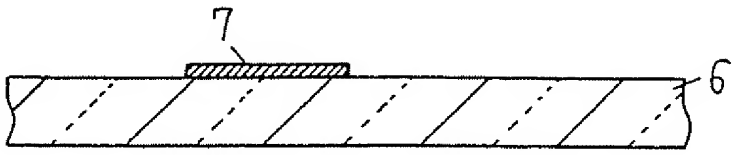


Fig.7B

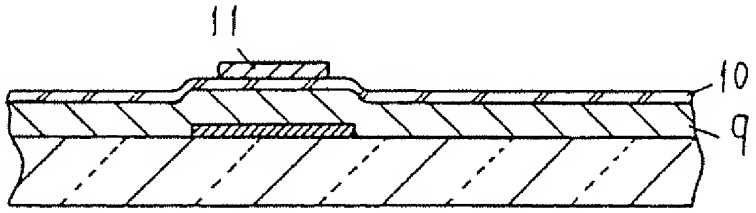


Fig.7C

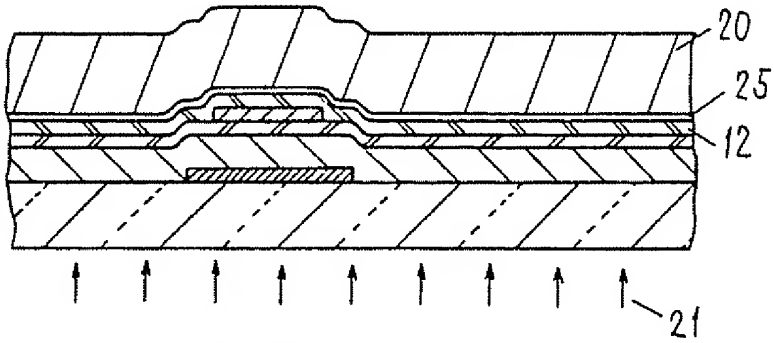


Fig.7D

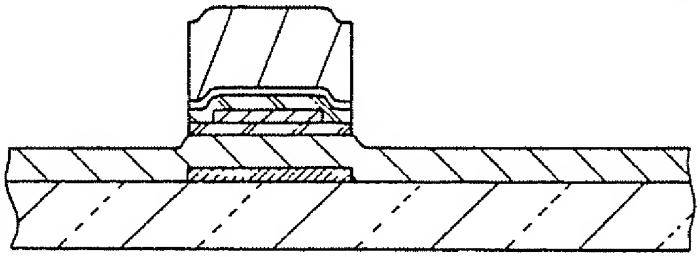


Fig.7E

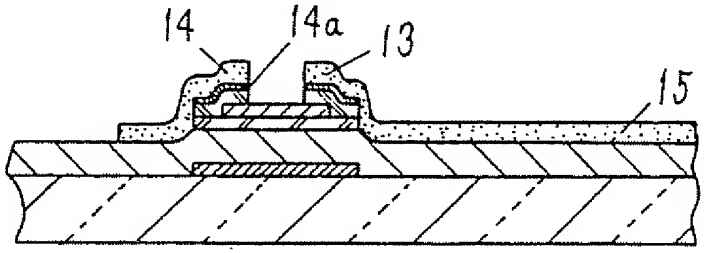
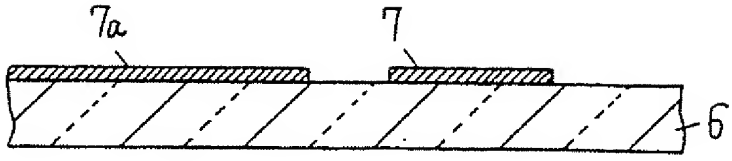


Fig.8A



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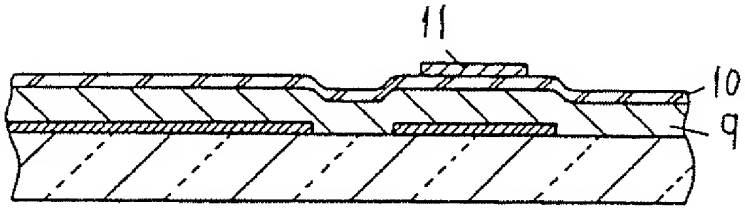


Fig.8C

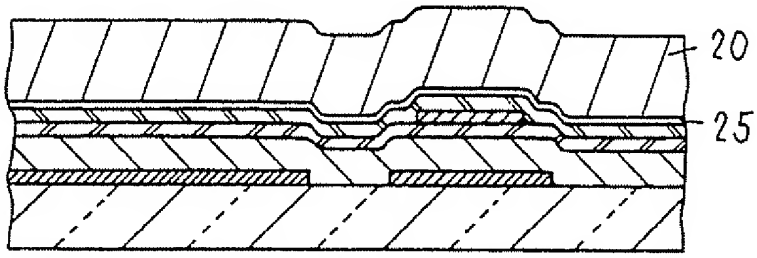
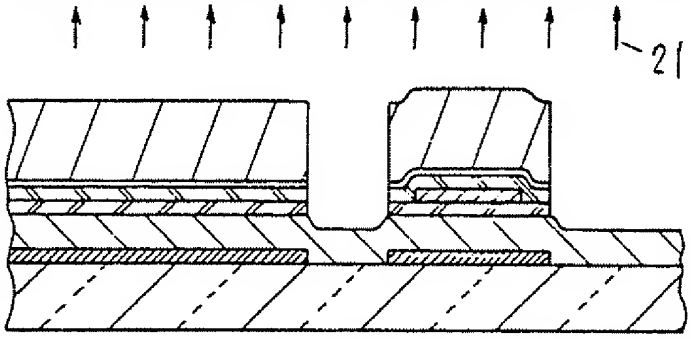


Fig.8D



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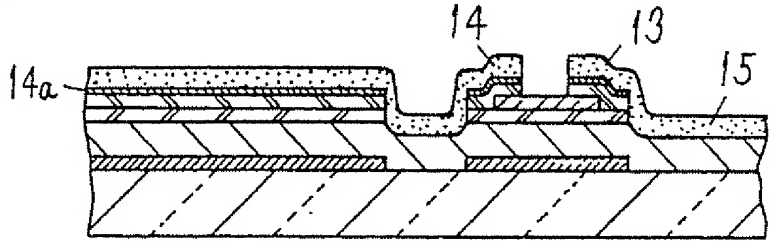

Fig. 9A

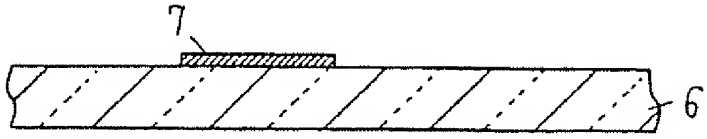

Fig. 9B

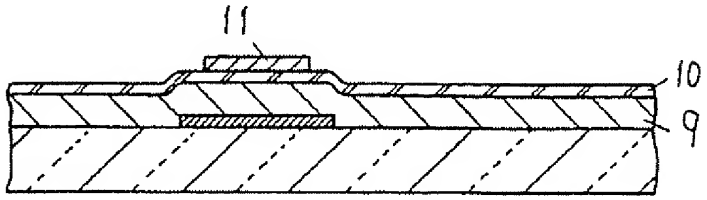

Fig. 9C

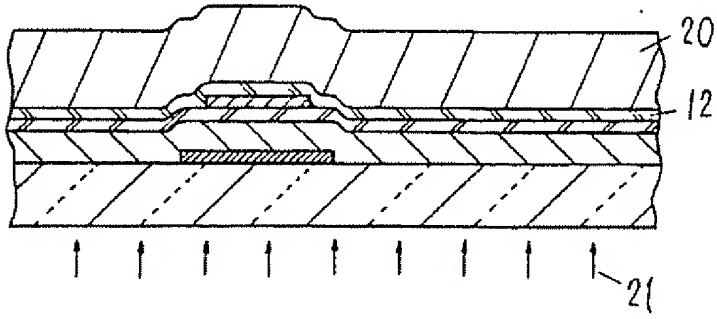

Fig. 9D

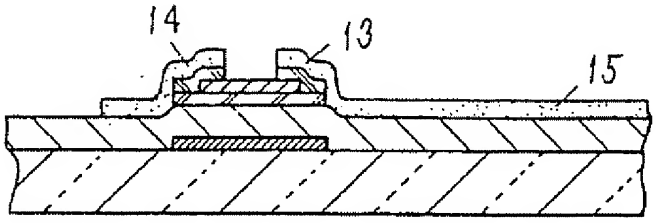

Fig. 9E

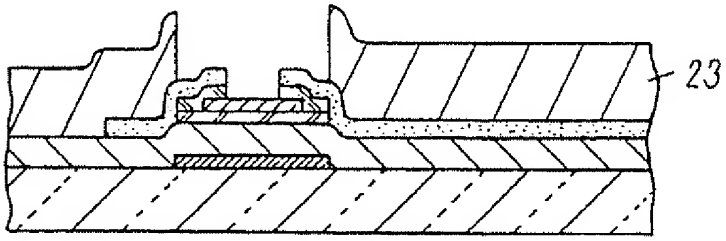

Fig. 9F

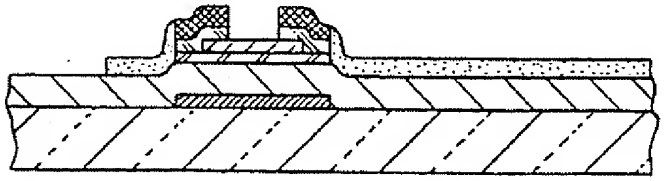

Fig.10A

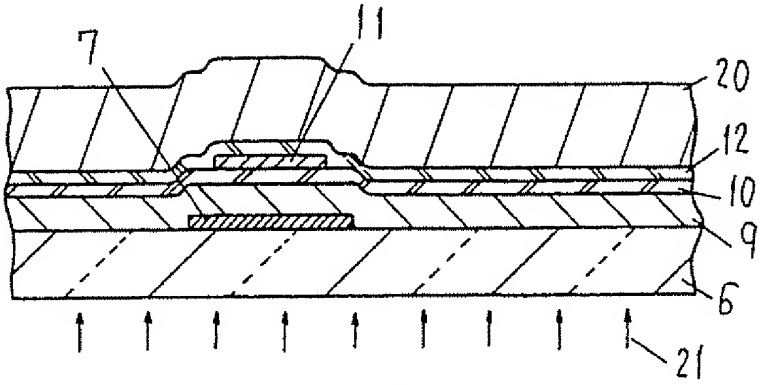

Fig.10B

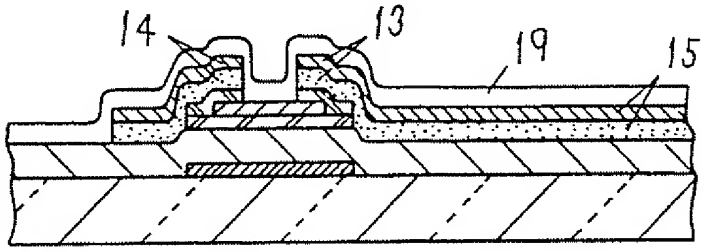

Fig.10C

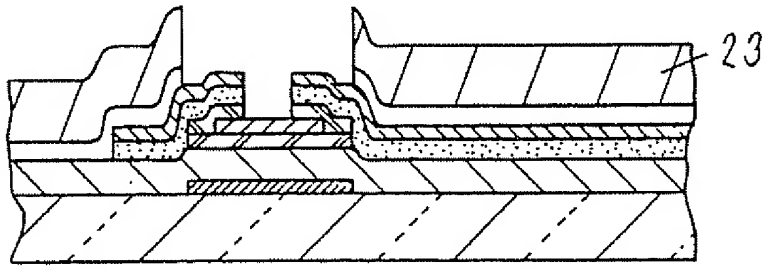

Fig.10D

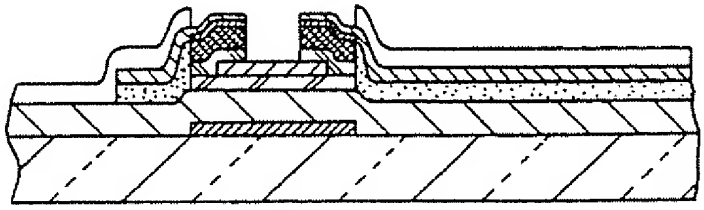

FIG. 11

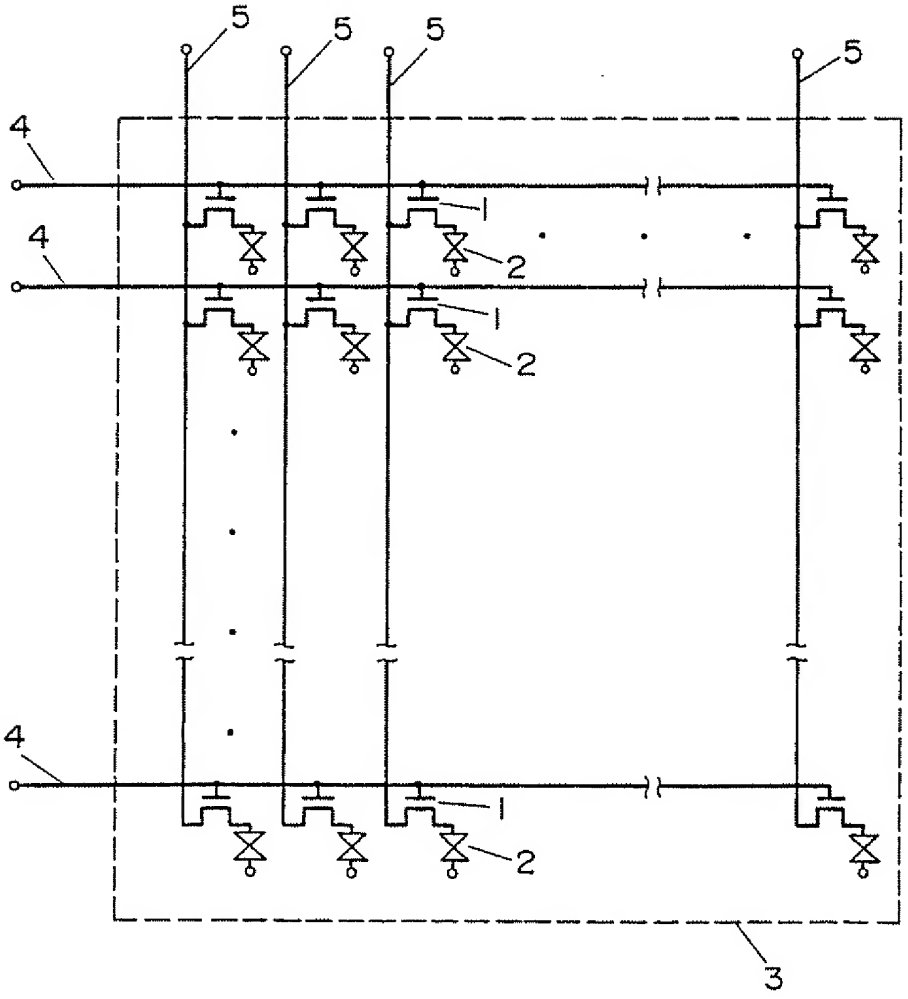

Fig. 12 A

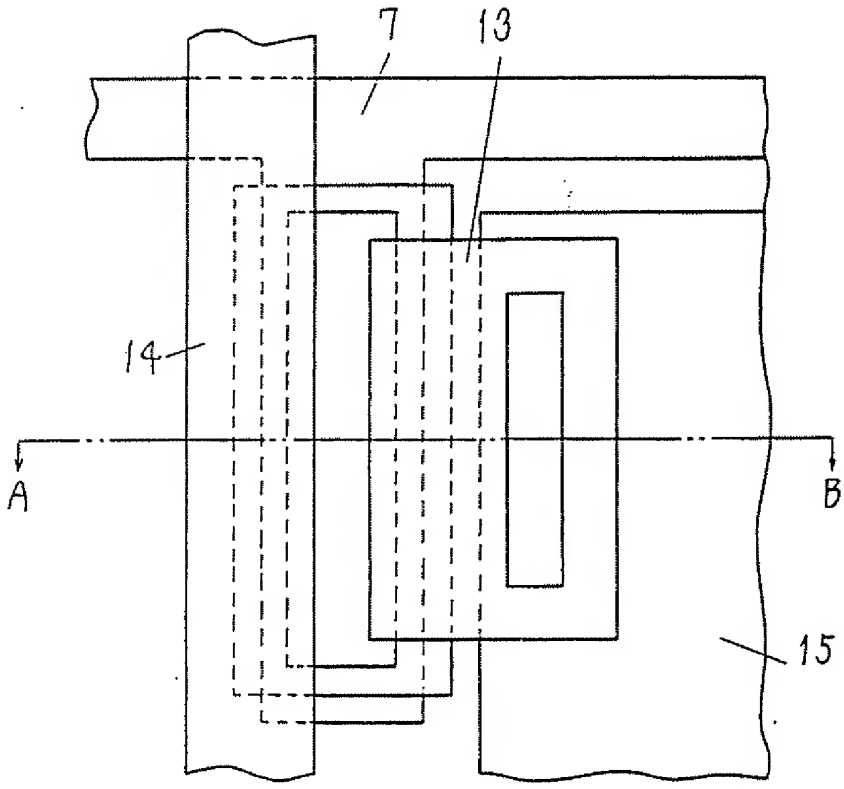

Fig. 12 B

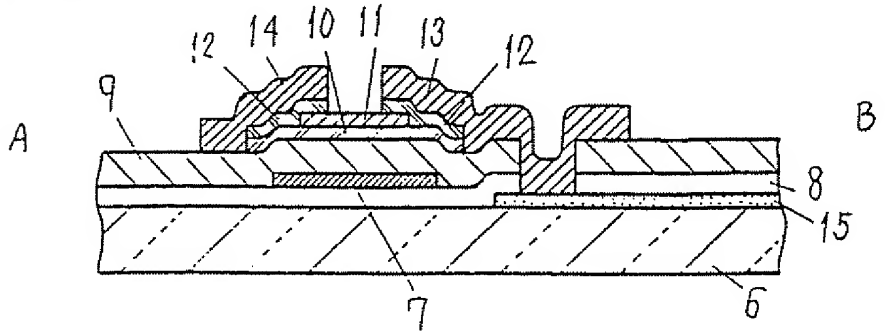

Fig. 13